In the Claims:

- 1-21. (Cancelled)
- 22. (Currently Amended) A semiconductor structure from which a strained channel transistor may be fabricated, comprising:
 - a semiconductor substrate;
- a first crystalline layer on the substrate, wherein the first crystalline layer and the substrate have a first lattice mismatch;
- a second crystalline layer on the first <u>crystalline</u> layer, <u>wherein the second crystalline</u> layer and first crystalline layer have a second lattice mismatch, the second lattice mismatch being greater than the first lattice mismatch;
 - a trench formed in the second crystalline layer; and
- a top epitaxial layer on the second <u>crystalline</u> layer, <u>wherein the top epitaxial layer and the second crystalline layer have a third lattice mismatch</u>, the third lattice <u>mismatch</u> being greater than the second lattice <u>mismatch</u>.
- 23. (Original) A semiconductor structure as in Claim 22, wherein upper and lower corners of the trench are rounded.
- 24. (Original) A semiconductor structure as in Claim 22 wherein upper corners of the trench are rounded.
- 25. (Original) A semiconductor structure as in Claim 23, wherein the radii of the corners are from about 5 to about 50 nm.

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- 26. (Original) A semiconductor structure as in Claim 22, wherein the trench has a depth of about 6,000 Å or less.
- 27. (Original) A semiconductor structure as in Claim 23, wherein the rounded corners are formed by heating the second layer in a gaseous ambient.
- 28. (Original) A semiconductor structure as in Claim 27, wherein heating is effected at a temperature within the range of about 700 C to about 950 C.
- 29. (Original) A semiconductor structure as in Claim 27, wherein the gaseous ambient includes O, H, N, He, Ne, Ar, Xe or a combination thereof.
- 30. (Original) A semiconductor structure as in Claim 27, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.
- 31. (Original) A semiconductor structure as in Claim 22, wherein the trench contains an insulative material comprising silicon oxide.
- 32. (Original) A semiconductor structure as in Claim 22, wherein the top layer is less than about 250 Å thick.
- 33. (Original) A semiconductor structure as in Claim 22, wherein the first, second and top layers comprise Si, Ge, C, or a compound semiconductor.
- 34. (Original) A semiconductor structure as in Claim 22, wherein the first, second and top layers comprise Si and Ge.

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35-36. (Cancelled)

- 37. (Original) A semiconductor structure as in Claim 22, wherein a free surface of one or more of the layers is planarized before a next superjacent layer is present thereon.
- 38. (Original) A semiconductor structure as in Claim 37, wherein planarization is effected by CMP.

39-59. (Cancelled)

60-89. (Cancelled)

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- 90. (New) A semiconductor structure, comprising:
 - a semiconductor substrate;
- a first crystalline layer on the substrate, wherein the first crystalline layer and the substrate have a first lattice mismatch;
- a second crystalline layer on the first crystalline layer, wherein the second crystalline layer and first crystalline layer have a second lattice mismatch;
 - a trench formed in the second crystalline layer; and
- a top epitaxial layer on the second crystalline layer, wherein the top epitaxial layer and the second crystalline layer have a third lattice mismatch, the third lattice mismatch being greater than the first and second lattice mismatch.
- 91. (New) A semiconductor structure as in Claim 90, wherein upper and lower corners of the trench are rounded.
- 92. (New) A semiconductor structure as in Claim 90, wherein upper corners of the trench are rounded.
- 93. (New) A semiconductor structure as in Claim 91, wherein the radii of the corners are from about 5 to about 50 nm.
- 94. (New) A semiconductor structure as in Claim 90, wherein the trench has a depth of about 6,000 Å or less.
- 95. (New) A semiconductor structure as in Claim 91, wherein the rounded corners are formed by heating the second layer in a gaseous ambient.

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- 96. (New) A semiconductor structure as in Claim 95, wherein heating is effected at a temperature within the range of about 700 C to about 950 C.
- 97. (New) A semiconductor structure as in Claim 95, wherein the gaseous ambient includes 0, H, N, He, Ne, Ar, Xe or a combination thereof.
- 98. (New) A semiconductor structure as in Claim 95, wherein heating is effected at a pressure within the range of about 10 to about 1,000 Torr.
- 99. (New) A semiconductor structure as in Claim 90, wherein the trench contains an insulative material comprising silicon oxide.
- 100. (New) A semiconductor structure as in Claim 90, wherein the top epitaxial layer is less than about 250 Å thick.
- 101. (New) A semiconductor structure as in Claim 90, wherein the first crystalline, second crystalline and top epitaxial layers comprise Si, Ge, C, or a compound semiconductor.
- 102. (New) A semiconductor structure as in Claim 90, wherein the first crystalline, second crystalline and top epitaxial layers comprise Si and Ge.
- 103. (New) A semiconductor structure as in Claim 90, wherein a free surface of one or more of the layers is planarized before a next superjacent layer is present thereon.

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